Remarks:

This amendment is submitted in an earnest effort to advance this case to issue without delay. The examiner has indicated that the case contains allowable subject matter.

The drawing has been amended to add the legend "Prior Art" to FIGS. 1-9 and to clean up the image. No new matter has been added.

The claims have been amended to eliminate the reference characters. Since this has, frankly, made the claims very hard to read and follow, a clean version of them is reproduced below:

1. (previously presented) A method for fine synchronization of a digital telecommunication receiver, comprising a code tracking process for maintaining fine alignment between an incoming spread spectrum signal and a locally generated code, said method comprising:

storing a plurality of consecutive samples of said incoming spread spectrum signal in a delay line;

determining by interpolation between consecutive samples of said incoming spread spectrum signal, by means of a first digitally controlled interpolator, an interpolated early sample anticipating an optimal sampling time instant;

determining by interpolation between consecutive samples of said incoming spread spectrum signal, by means of

a second digitally controlled interpolator, an interpolated middle sample corresponding to said optimal sampling time instant;

determining by interpolation between consecutive samples of said incoming spread spectrum signal, by means of a third digitally controlled interpolator, an interpolated late sample delayed with respect to said optimal sampling time instant;

calculating an error signal as the difference between the energy of the symbols computed from said interpolated early and late samples; and

generating, from said error signal, a control signal for controlling the interpolation phase of said second digitally controlled interpolator;

wherein the step of generating a control signal comprises:

extracting the sign of said error signal;

accumulating said sign of said error signal for the generation of an intermediate control signal;

calculating the absolute value of said error signal at a time instant n;

comparing said absolute value of said error signal at said time instant n with the absolute value of said error signal at a previous time instant n-1; and

updating said control signal to the value of said intermediate control signal if the absolute value of said error signal at time n is smaller than the absolute value of the same error signal at time n-1, maintaining otherwise unchanged the value of said control signal.

2. (previously presented) The method according to claim 1, wherein said step of accumulating said sign of said error signal provides that the value accumulated has a positive saturation value of +4 and a negative saturation value of -4.

3. (previously presented) The method according to claim 1, wherein said step of comparing said absolute value of said error signal comprises:

storing the absolute value of said error signal in a first register, maintaining such absolute value in said register at least until a new absolute value of said error signal has been calculated; and

comparing said new absolute value of said error signal with the absolute value stored in said first register, and storing said new absolute value in said first register, overwriting the absolute value previously stored.

4. (previously presented) The method according to claim 1, wherein said step of updating said control signal comprises:

storing the value of a previous control signal in a second register, maintaining such value in said second register at least until a new value of said intermediate control signal has been calculated; and

overwriting the value of said control signal stored in said second register with the new value of said intermediate control signal if the absolute value of said error signal at time n is smaller than the absolute value of

the same error signal at time n-1, maintaining otherwise unchanged the value stored in said second register.

5. (previously presented) A digital communication receiver comprising a device for maintaining fine alignment between an incoming spread spectrum signal and a locally generated code, said device comprising:

a delay line for storing a plurality of consecutive samples of said incoming spread spectrum signal;

a first digitally controlled interpolator for determining by interpolation between consecutive samples stored in said delay line an interpolated early sample anticipating an optimal sampling time instant;

a second digitally controlled interpolator for determining by interpolation between consecutive samples stored in said delay line an interpolated middle sample corresponding to said optimal sampling time instant;

a third digitally controlled interpolator for determining by interpolation between consecutive samples stored in said delay line an interpolated late sample delayed with respect to said optimal sampling time instant;

at least one correlator for calculating an error signal as the difference between the energy of the symbols computed from said interpolated early and late samples; and

a circuit for generating a control signal for controlling the interpolation phase of said second digitally controlled interpolator;

wherein the means for generating a control signal comprises:

a circuit for extracting the sign of said error signal;

a circuit for accumulating said sign of said error signal in a register, for the generation of an intermediate control signal;

a circuit for calculating the absolute value of said error signal at a time instant n;

at least a comparator for comparing said absolute value of said error signal at said time instant n with the absolute value of said error signal at a previous time instant n-1; and

a controllable switch for updating said control signal to the value of said intermediate control signal if the absolute value of said error signal at time n is smaller than the absolute value of the same error signal at time n-1, maintaining otherwise unchanged the value of said control signal.

6. (previously presented) The digital communication receiver according to claim 5, wherein said register in which is accumulated the sign of said error signal has a positive saturation value of +4 and a negative saturation value of -4.

7. (previously presented) The digital communication receiver according to claim 5, wherein said at least one comparator for comparing said absolute value of said error signal comprises:

a first register for storing the absolute value of said error signal at a time instant n-1, maintaining such absolute value in said register at least until a new absolute value of said error signal has been calculated; and

a comparator for comparing said new absolute value of said error signal with the absolute value stored in said first register, generating a signal indicating whether said new absolute value is smaller than the previously stored absolute value.

8. (previously presented) The digital communication receiver according to claim 7, wherein said controllable switch for updating said control signal comprises:

a second register for storing the value of a previous control signal , maintaining such value in said register at least until a new value of said intermediate control signal has been calculated; and

a switch, controlled by the signal generated by said comparator, for storing in said second register a new value of said control signal, if said new absolute value is smaller than the previously stored absolute value, or for leaving unaltered the value stored in the same register if such condition is not verified.

Thus all of the objections have been overcome so that the case is in condition for allowance and passage to issue. Notice to that effect is earnestly solicited.

If only minor problems that could be corrected by means of a telephone conference stand in the way of allowance of this case, the examiner is invited to call the undersigned to make the necessary corrections.

K.F. Ross P.C.

/Andrew Wilford/

by: Andrew Wilford, 26,597
Attorney for Applicant

22 October 2008
5683 Riverdale Avenue Box 900
Bronx, NY 10471-0900
Cust. No.: 535
Tel: 718 884-6600
Fax: 718 601-1099
Email: *email@kfrpc.com*

Enclosure: Replacement drawing (8 sheets)